## REMARKS

Claims 1-23 are pending in this application. By this Amendment, claims 1, 5, 14, and 17 are amended, and claims 20-23 are new.

The courtesies extended to Applicant's representative by Examiner Tan at the telephone interview held October 4, are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below and constitute Applicant's record of the interview.

### I. Rejection of Claims 1, 4, 5, 8 and 14

Claims 1, 4, 5, 8, 14 and 17 are rejected under 35 U.S.C. §013(a) as being unpatentable over U.S. Patent 6,034,563 to Mashiko (hereinafter "Mashiko") in view of U.S. Patent 5,097,151 to Eerenstein et al. (hereinafter "Eerenstein"). We respectfully traverse this rejection.

The Office Action asserts that Mashiko discloses the claimed features as shown in Figures 9-18, a semiconductor circuit, comprising: a plurality of circuit blocks capable of transitions from an operating state to a standby state and from a standby state to an operating state; and, a control circuit which controls, in event-driven fashion, the back-gate voltages of transistors forming logic elements of said circuit blocks.

Referring to Fig. 9 of Mashiko which discloses transistor Q1 located between the logic circuit 11 and the potential line VDDV, and the transistor Q2 located between the logic circuit 11 and the potential line GNDV. Mashiko intends to decrease the leakage current through the transistor Q1 or Q2 which effectively turns off the logic circuit 11 when in a standby mode. (Col. , lines 40-42). Mashiko does not teach controlling the back-gate voltage of the transistors forming logic elements provided in the circuit blocks (Fig. 3). Controlling the back-gate voltage of the transistors forming logic elements provided in the circuit blocks in event-driven fashion is a distinctive feature of the present invention. That is to say, the

present invention does not necessarily require turning off the logic elements provided in the circuit blocks as compared to Mashiko. The present invention enables a control circuit to keep supplying power to the logic elements provided in the circuit blocks. Mashiko does not teach or suggest the feature of the present invention. Furthermore, Mashiko does not teach or suggest the control circuit which controls, in event-driven fashion, the back-gate voltages of transistors forming logic elements of said circuit blocks, based on the finite state machine that stipulates in advance each of the state transistors of said plurality of circuit blocks. According to the present invention, fine grain division by functions into numerous circuit blocks can precisely control the leakage currents of individual circuit blocks, so that the leakage current of the entire semiconductor integrated circuit can be greatly reduced.

Based on the discussion above, we believe independent claims 1, 5, 14, 17 and 20 are in condition for allowance. We respectfully request the Examiner reconsider and withdraw the rejections.

Anticipated acceptance of independent claims 1, 5, 14, 17 and 20 based on the discussion presented herein, it is respectfully requested that the rejection of the corresponding dependent claims be reconsidered and withdrawn.

## II. Allowable Subject Matter

Claims 9-12 are objected to as being dependent upon a rejected base claim. Anticipating acceptance of independent claim 1 based on the discussed presented herein, it is requested that this objection be reconsidered and withdrawn.

## III. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of all claims is earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

10/26/05

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